A Survey on Implementation of Vedic Mathematics Sutras in Information Technology

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Abstract

Vedic mathematics is a powerful tool for fast and efficient computational purposes in the area of information technology. The implementation of various Vedic sutras reduces the time taken for computation in the field of Computer Science, Digital Signal Processing and various applications in Cryptography and Communication. In the field of information technology, the different applications need large computation capacity and large amount of energy. So to reduce the complexity, we need to select appropriate Vedic sutras and then implement them appropriately.

This survey is aimed at assessing the implications of different Sutras used in various applications of computer science. The results show that, on implementation of appropriate Vedic Ssutras for computational purposes, the accuracy, efficiency, speed and power consumption drastically changes in a positive way, as compared with the traditional computational methods.

Keywords: Vedic Mathematics, Information Technology

Introduction

The term Vedic mathematics refers to a set of sixteen mathematical sutras and their corollaries derived from the Vedas. The Vedas are ancient texts written in Sanskrit; the word Veda means “knowledge” – knowledge both within and beyond the senses. It is conjectured that the Vedic mathematical system was part of the Sulvasutras. This is a system of calculations based on easy-to-follow rules and principles that can be used effectively to solve problems in arithmetic, algebra, geometry and trigonometry. The Vedic system was rediscovered between 1911 and 1918 by Sri Swami Bharati Krisna Tirthaji. The applications of Vedic sutras in Information Technology help improve the computation time, reducing the power consumption and improves the efficiency as compared with the traditional methods. The literature survey is organized as the literature review in Section II and the conclusion part in session III.

Section II Literature Survay

Surabhi Jain et.al [1] propose the Deconvolution Algorithm based on Vedic mathematics.They have implemented an optimized binary division architecture using the Nikhilam and Paravartya sutras. Using these sutras in the deconvolution algorithm reduces its iteration and improves results of time delay and with less complexity. The proposed division algorithm is coded in Verilog, Synthesized and Simulated using Xilinx ISE design suit 14.2. The simulated result shows a reduction in delay compared to the conventional method.

Richa Sharma et.al [2] proposed the design of high speed multiplier and squaring architectures based upon Vedic mathematics. In the existing methods of the Vedic multiplier architecture the partial product terms are computed in parallel and then added at the end to get the final result. In the proposed work all the partial products are adjusted using a concatenation operation and are added using a single carray save adder, instead of two adders at different stages. The reduced number of computations in multiplication, due to adjustments using concatenation operation and one carry save adder only, offers a significant improvement in speed to the designed multiplier.

In the paper [3], Design of High Performance 8 bit Vedic multiplier using Compressor, Radhashyam et.al propose the design of a high speed Vedic multiplier using the compressor based on Vedic mathematics that has improved the performance of the multiplier.

Shashank et.al [4] provides a comparative study of the Vedic multiplier using CMOS, PFAL and ECRL. By using the Vedic multiplication, generation of partial sums and products are achieved in a single step with the help of an adiabatic approach that helps in realizing the high speed and low power operation of the binary Vedic design. They simulated the designs using Cadence Virtuoso tool using 180 nm CMOS technology and the simulation result shows PFAL is the best compared to the other technology (CMOS, ECRC).

Prabi Saha et.al [5] presented a high speed complex multiplier design (ASCI) using Vedic mathematics. By using Vedic methods the partial products and sums are generated in one step which reduces the carry propagation from LSB to MSB as well as a reduction in propagation delay compared to other methods.

Surabhi Jain et.al propose [6] Digital Signal Processing which is used in many areas of Electrical Engineering. In digital signal processing and image processing discrete convolution is central to many applications. The components required for implementation of convolution calculation are adder and multiplier for partial multiplication. This process affects the overall speed and is time consuming. They propose a new method using Vedic mathematics to overcome all these problems. The Urdhva Tiryagbhyam and Nikilam algorithams are used for the purpose. The simulated result shows a reduction in time delay compared to the conventional method.

In the paper, Multiplier Design Based on Ancient Indian Vedic Mathematics, Honey Durga Tiwari et.al propose [7] a new multiplier and square architecture based on the Urdhva Tiryagbhyam (Vertically and Crosswise) sutra for low power and high speed applications.

Kunal Jadhav et.al propose [8] a Vedic algorithm technique used for faster execution of an arithmetic module of an ALU. Urdhva Tiryagbhyam is again used for this purpose. By implementing this algorithm a faster way to get the output with fewer logical elements is involved, thereby reducing the delay, while effectively increasing the speed of processing the output.

Kbiraj Sethi et.al propose [9] a high speed squaring circuit for binary numbers using a Vedic multiplier. Using only one Vedic multiplier and one squaring circuit twice in their study for better performance in terms of speed.

P.K Srimani et.al published a comparative study of [10] Fast Matrix Multiplication Methods (FMMM) by using Vedic algorithms. In this study they compare the fast matrix multiplication using Vedic algorithms with the classical methods like standard methods, Strassens and the Winograd Method. Vedic algorithms perform better in reduction in the time complexity compared to the above-mentioned methods.

In 2010 Ashish Raman et.al proposed [11] a Reconfigurable Fast Fourier Transform design using Vedic multiplier with high speed. In this method the Urdhava Triyagbhyam algorithm is used for improving efficiency. This method is implemented as an FPGA based system and the reconfigurable FFT has high speed and small area as compared to the conventional FFT.

Pradeep M C et.al [12] propose a low power and high-speed multiplier architecture also using the Urdhava Triyagbhyam sutra to improve the performance of CPU. In this method the simulated result shows better performance and significant amount of power reduction.

Dani George et.al propose [13] an efficient design and implementation of RSA encryption system using an encoded multiplier. Implementation of their method using Vedic mathematics along with encoder multiplier architecture in the RSA algorithm makes the encryption system more efficient. The RSA encryption and decryption is done in Verilog Tool.

Conclusion

This paper reviews the different Vedic Sutras that are implemented for reducing speed and power consumption and increasing efficiency. The majority of the work depends on the Nikhilam and Urdhva Tiryagbhyam sutras. It appears that the Vedic mathematics sutras help develop new algorithms for improving all areas, including Digital Signal Processing and Image Processing.

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