COMPARATIVE STUDY OF ADDERS USED IN DESIGNING HIGH SPEED VEDIC MULTIPLIERS FOR VLSI APPLICATIONS

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Abstract

Fast and low power consuming systems are the need of the current technology. Design and development of low power Microcontroller applications and Digital Signal Processors (DSP) which work at a very high speed is a challenging task. The speed of a Digital Signal Processor is directly dependent on the speed of the multiplier. In order to achieve the required performance in many real-time applications, maintaining higher throughput in arithmetic operations plays an important role. The performance of a multiplier depends on the adder used in logic circuits. Vedic Mathematics provides one of the fastest multiplier algorithms. This paper presents a comparative study of Vedic multiplier based on different adders.

Keywords

Digital Signal Processor, Vedic mathematics, Vedic multiplier, VLSI.

Introduction

In several DSPs for performing operations like convolution, filtering, Fast Fourier Transforms (FFT) and in the ALU units, multiplication is the most fundamental operation [1]. Multiplication dominates the computational requirements of DSP [2] systems, marking the need for a high speed multiplier system that is efficient in terms of power considerations as well. Over the years, as a result of expanding signal and computer processing applications, the demand for high speed processing has seen a constant increase. Arithmetic operations with higher throughput are essential to achieve the required performance in many real-time signals. For many applications, the reduction of power consumption and speed forms an essential requirement.

Digital Multipliers

A binary multiplier, used in digital electronics, is an electronic circuit to multiply two binary numbers. It is constructed using binary adders. Some of the types of multipliers are serial multipliers and parallel multipliers. The differenet multipliers in use are Braun Multiplier, Combinational Multiplier, Booth Multiplier, Modified Booth Multiplier, Baugh - Wooley Multiplier, Dadda Multiplier, Wallace-tree multiplier [3].

Adders

Addition is a basic fundamental operation for any digital system [4]. The extensive use of adders for basic digital operations such as addition, subtraction, multiplication and division make them a very important component of digital systems. Hence, enhancing the performance of an adder influences the performance of other operations and, in turn, the digital system. There are different adders used in digital circuits namely Ripple Carry adder, Carry Look Ahead adder, Carry Save adder, Carry Skip adder, Carry Select adder, Manchester adder, etc. Multiplication in digital systems incorporates either an individual or combinations of these adders to achieve faster results.

Vedic Mathematics

Vedic Mathematics is the name given to the ancient system of Indian Mathematics which was rediscovered from the Vedas between 1911 and 1918 by Sri Bharati Krsna Tirthaji (1884-1960). According to his research all of mathematics is based on sixteen Sutras, or word-formulae [5,6].

Number Systems

Human thinking is acquainted with the decimal number system. Almost everyone is familiar with this system using ten digits [7]. However, digital devices, especially computers, use the binary number system instead of decimal, using two digits, that is, 0 and 1. Various other number systems also use this fundamental concept of the decimal number system, for example, quaternary, senary, octal, duodecimal, quadrodecimal, hexadecimal and vigesimal number system using four, six, eight, twelve, fourteen, sixteen, and twenty digits, respectively.

Vedic mathematics sutras are currently known to be easily applicable to the decimal number system. For it to be applicable to digital systems, it is necessary to establish the correlation of sutras with the number systems adopted by the binary system.

Digital system operations are based on the principles of binary number system. By grouping consecutive 4 bits from the right-hand side of a given binary number, hexadecimal numbers are obtained. Even the physical address locations, operands (multiplicand, multipliers etc.,) are represented in Hexadecimal numbers in assembly level programming used in microprocessors. By carefully observing the binary, hexadecimal number systems and their multiplication tables given in the Dozenal Society of America [8], inferences can be drawn leading to applications of Vedic mathematics sutras to the Hexadecimal number system. This will lead to a different perspective for implementing Vedic mathematical sutras into digital systems as demonstrated by the following examples.

Example: 1111 1111 = FF H, 1101 x 1001 = E x 9, FFE x 12C

In the Hexadecimal number system the terminologies used are:

Terminology	Number Of Bits	Binary representation	Hexadecimal representation
Nibble	4	1010	A
Byte	8	**1001**1110	**9**E
Word	16	**1011**1100**0001**0010	**BC1**2

Nikhilam sutra :

Decimal :	6 x 9 = 54	74 x 99 = 7326
Hexadecimal	4 x F = 3C	23 x FF = 22DD
	7 x F = 69	39 x FF = 38C7
	C x F = B4	AC x FF = AB54
	F x F = E1	FF x FF = FE01

Nikhilam sutra

Yaavadunam	**Ekadhikena**	**Antyayordashake api**
$9^2 = (9-1)/1^2 = 81$	$25^2 = (2 \times 3)/5^2 = 625$	34 x 36 = (3x4)/(4x6) = 1224
$F^2 = (F-1)/1^2 = E1$	$18^2 = (1 \times 2)/8^2 = 340$	2E x 22 = (2 x 3)/(Ex2) = 61C
$D^2 = (D-3)/3^2 = A9$	$28^2 = (2 \times 3)/8^2 = 640$	4F x 41 = (4 x 5)/ (Fx1) = 140F
$C^2 = (C-4)/4^2 = 90$	$38^2 = (3 \times 4)/8^2 = C40$	7C x 74 = (7 x 8)/(Cx4) = 3830
$A^2 = (A-6)/6^2 = 64$	$A8^2 = (A \times B)/8^2 = 6E40$	BD x B3 = (B x C)/(D x 3) = 8427

Nikhilam					**Vertically & Crosswise**	
8 – **2** 7 – **3**	E **-2** D **-3**	A **-6** C **-4**	F4 – **0C** FD – **03**	D3 - **2D** B8 - **48**	23 21	E2 33
56	**B6**	**$6_1$8 = 78**	**F124**	**$8B_CA8$ = 97A8**	**483**	**2D06**

Observations and Conclusion

Vedic maths sutras are also applicable to Hexadecimal number system. The adders used in the current system use the Shift and add method for multiplication. By suitably combining the Compare, Complement, Shift and add methods, it should be possible to design adders that would

perform in a better way by utilizing lesser clock cycles for computation. In turn, better multipliers can be designed which further enhances the performance of the digital system in a way opening new avenues for Vedic digital research resulting into true green computing.

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